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EXAMINER	
BODDIE, WILLIAM	

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2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/648,153	KOYAMA, JUN	
	Examiner	Art Unit	
	WILLIAM L. BODDIE	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,8-14,17-22,24-27,29,47-50 and 55-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,8-14,17-22,24-27,29,47-50 and 55-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/11/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *See Continuation Sheet*.

Continuation of Attachment(s) 6). Other: copy/translation of Hoshi reference.

DETAILED ACTION

1. In an amendment dated, August 12th, 2010, the Applicant amended claims 6, 12, 18, 24, 55, 57 and cancelled claims 7 and 23. Currently claims 6, 8-14, 17-22, 24-27, 29 and 47-50 and 55-59 are pending.

Allowable Subject Matter

2. The indicated allowability of claims 7 and 23 is withdrawn in view of the newly presented reference of Hoshi. Rejections based on the newly cited reference follow.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 18-19, 22 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parks (US 5,471,225) in view of Hoshi (JP 58-143389).

With respect to claim 18, Parks discloses, an active matrix display device (fig. 2; col. 3, lines 17-19) having an electro-optical modulating layer (40 in fig. 3) disposed between a pair of substrates (24 and 22 in fig. 2), said active matrix display device comprising:

a plurality of column lines (32 in fig. 5) and a plurality of row lines (34 in fig. 5) supported by one of the substrates (fig. 3) and defining a plurality of pixels in a matrix form (fig. 5);

a plurality of pixel electrodes formed in said plurality of pixels (36 in fig. 5) and supported by said one of said substrates (fig. 3);

a first thin film transistor (col. 3, lines 6-8) disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines (38 in fig. 5);

a memory circuit (52, 54, R1-2 in fig. 5) disposed in each of said pixels and electrically connected to said thin film transistor (fig. 5), wherein said memory circuit stores an information output by said thin film transistor (col. 6, lines 5-18); and

at least two voltage source lines electrically connected to said memory circuit (Power and ground voltages in fig. 5),

an opposite electrode on the other of said substrates (30 in fig. 3, for example)

wherein different voltages are applied to said pixel electrodes through said at least two voltage source lines based on the information stored by the corresponding memory circuit (col. 6, lines 5-18, 52-61); and

wherein said memory circuit comprises at least two inverters (52, 54, R1-2 in fig. 5), said inverters comprising at least two thin film transistors and being connected with said voltage source lines (fig. 5).

Parks does not expressly disclose wherein an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode.

Hoshi discloses, wherein an AC voltage (12a in fig. 3a) having an amplitude equivalent to that of the voltages output of the memory circuit (12b in fig. 3b; both have

an amplitude of V) is supplied to the opposite electrode (fig. 2; 8th line from bottom of page 5 of provided translation).

Hoshi and Parks are analogous art because they are both from the same field of endeavor namely LCD device control and driving.

At the time of the invention it would have been obvious to one of ordinary skill in the art to apply the AC voltage as taught by Hoshi for the benefit of reduced power consumption (Hoshi; middle of page 6).

With respect to claim 19, Parks and Hoshi disclose, the active matrix display device of claim 18 (see above).

Parks further discloses, wherein the number of pixel electrodes equals the number of the digital memory circuits (clear from fig. 5).

With respect to claim 22, Parks and Hoshi disclose, the active matrix display device of claim 18 (see above).

Parks, further discloses, wherein the different voltages include a high voltage and a low voltage (fig. 5, power and ground are seen as a high and low voltage).

With respect to claim 49, Parks and Hoshi disclose, the active matrix display device according to claim 18 (see above).

Parks further discloses, wherein said electro-optical modulating layer comprises a liquid crystal (title).

5. Claims 6, 8, 11, 47, 55-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parks (US 5,471,225) in view of Runaldue et al. (US 5,325,338) and further in view of Hoshi (JP 58-143389).

With respect to claim 6, Parks discloses, an active matrix display device (fig. 2; col. 3, lines 17-19) having an electro-optical modulating layer (40 in fig. 3) disposed between a pair of substrates (24 and 22 in fig. 2), said active matrix display device comprising:

a plurality of column lines (32 in fig. 5) and a plurality of row lines (34 in fig. 5) supported by one of the substrates (fig. 3) and defining a plurality of pixels in a matrix form (fig. 5);

a plurality of pixel electrodes formed in said plurality of pixels (36 in fig. 5) and supported by said one of said substrates (fig. 3);

a thin film transistor (col. 3, lines 6-8) disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines (38 in fig. 5);

a memory circuit (52, 54, R1-2 in fig. 5) disposed in each of said pixels and electrically connected to said thin film transistor (fig. 5), wherein said memory circuit stores an information output by said thin film transistor (col. 6, lines 5-18); and

at least two voltage source lines electrically connected to said memory circuit (Power and ground voltages in fig. 5); and

an opposite electrode on the other of said substrates (30 in fig. 3, for example),

wherein different voltages are applied to said pixel electrodes through said at least two voltage source lines based on the information stored by the corresponding memory circuit (col. 6, lines 5-18, 52-61); and

wherein said memory circuit comprises a pair of inverters connected to each other (fig. 5; col. 6, lines 52-61), each of said inverters comprising an N-channel TFT (fig. 5).

Parks does not expressly disclose each inverter comprising both an N-channel TFT and a P-channel TFT.

Runaldue discloses, a display memory circuit which comprises a pair of inverters connected to each other (100-103 in fig. 3), each of said inverters comprising an N-channel TFT (101 and 103 in fig. 3) and a P-channel TFT (100 and 102 in fig. 3).

Runaldue and Parks are analogous art because they are both from the same field of endeavor namely display control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the memory circuit of Parks with that of Runaldue.

The motivation for doing so would have been for the well-known advantage of reduced power consumption.

Neither Runaldue nor Parks expressly disclose wherein an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode.

Hoshi discloses, wherein an AC voltage (12a in fig. 3a) having an amplitude equivalent to that of the voltages output of the memory circuit (12b in fig. 3b; both have an amplitude of V) is supplied to the opposite electrode (fig. 2; 8th line from bottom of page 5 of provided translation).

Runaldue, Hoshi and Parks are analogous art because they are both from the same field of endeavor namely LCD device control and driving.

At the time of the invention it would have been obvious to one of ordinary skill in the art to apply the AC voltage as taught by Hoshi for the benefit of reduced power consumption (Hoshi; middle of page 6).

With respect to claim 8, Parks, Hoshi and Runaldue disclose, the active matrix display device of claim 6 (see above).

Parks further discloses, wherein the number of pixel electrodes equals the number of the digital memory circuits (clear from fig. 5).

With respect to claim 11, Parks, Hoshi and Runaldue disclose, the active matrix display device of claim 6 (see above).

Parks, further discloses, wherein the different voltages include a high voltage and a low voltage (fig. 5, power and ground are seen as a high and low voltage).

With respect to claim 47, Parks, Hoshi and Runaldue disclose, the active matrix display device according to claim 6 (see above).

Parks further discloses, wherein said electro-optical modulating layer comprises a liquid crystal (title).

With respect to claim 55, Parks discloses, a method of operating an active matrix display device comprising the steps of:

storing a data in a memory circuit provided at one pixel (50 in fig. 5; col. 6, lines 5-36); and

supplying a voltage to a pixel electrode (36 in fig. 5) of said pixel in accordance with the data stored in said memory circuit (col. 6, lines 2-5),

wherein said memory circuit comprises at least first and second inverters (52, 54, R1-2 in fig. 5), each of said inverters comprising an n-channel TFT (fig. 5) formed over a substrate (col. 6, lines 37-39).

Parks does not expressly disclose each inverter comprising both an N-channel TFT and a P-channel TFT.

Runaldue discloses, a display memory circuit which comprises a pair of inverters connected to each other (100-103 in fig. 3), each of said inverters comprising an N-channel TFT (101 and 103 in fig. 3) and a P-channel TFT (100 and 102 in fig. 3).

Runaldue and Parks are analogous art because they are both from the same field of endeavor namely display control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the memory circuit of Parks with that of Runaldue.

The motivation for doing so would have been for the well-known advantage of reduced power consumption.

each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate.

Neither Runaldue nor Parks expressly disclose wherein an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode.

Hoshi discloses, wherein an AC voltage (12a in fig. 3a) having an amplitude equivalent to that of the voltages output of the memory circuit (12b in fig. 3b; both have an amplitude of V) is supplied to the opposite electrode (fig. 2; 8th line from bottom of page 5 of provided translation).

Runaldue, Hoshi and Parks are analogous art because they are both from the same field of endeavor namely LCD device control and driving.

At the time of the invention it would have been obvious to one of ordinary skill in the art to apply the AC voltage as taught by Hoshi for the benefit of reduced power consumption (Hoshi; middle of page 6).

With respect to claim 56, Parks, Hoshi and Runaldue disclose, the method according to claim 55 (see above).

Parks further discloses, wherein an output terminal of said memory circuit is connected to said pixel electrode (fig. 5).

With respect to claim 57, Parks discloses, a method of operating an active matrix display device comprising the steps of:

storing a data through a switching thin film transistor (38 in fig. 5) provided at one pixel to a memory circuit (50 in fig. 5; col. 6, lines 5-36); and

supplying one of two voltages from two voltage source lines (power and ground in fig. 5) to a pixel electrode (36 in fig. 5) of said pixel in accordance with the data stored in said memory circuit (col. 6, lines 2-5),

wherein said memory circuit comprises at least first and second inverters (52, 54, R1-2 in fig. 5), each of said inverters comprising an n-channel TFT (fig. 5) formed over a substrate (col. 6, lines 37-39).

Parks does not expressly disclose each inverter comprising both an N-channel TFT and a P-channel TFT.

Runaldue discloses, a display memory circuit which comprises a pair of inverters connected to each other (100-103 in fig. 3), each of said inverters comprising an N-channel TFT (101 and 103 in fig. 3) and a P-channel TFT (100 and 102 in fig. 3).

Runaldue and Parks are analogous art because they are both from the same field of endeavor namely display control circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to replace the memory circuit of Parks with that of Runaldue.

The motivation for doing so would have been for the well-known advantage of reduced power consumption.

each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate.

Neither Runaldue nor Parks expressly disclose wherein an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode.

Hoshi discloses, wherein an AC voltage (12a in fig. 3a) having an amplitude equivalent to that of the voltages output of the memory circuit (12b in fig. 3b; both have

an amplitude of V) is supplied to the opposite electrode (fig. 2; 8th line from bottom of page 5 of provided translation).

Runaldue, Hoshi and Parks are analogous art because they are both from the same field of endeavor namely LCD device control and driving.

At the time of the invention it would have been obvious to one of ordinary skill in the art to apply the AC voltage as taught by Hoshi for the benefit of reduced power consumption (Hoshi; middle of page 6).

With respect to claim 58, Parks, Hoshi and Runaldue disclose, the method according to claim 57 (see above).

Parks further discloses, wherein an output terminal of said memory circuit is connected to said pixel electrode (fig. 5).

With respect to claim 59, Parks, Hoshi and Runaldue disclose, the method according to claim 57 (see above).

Parks further discloses, wherein said display device is a liquid crystal device (title).

6. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parks (US 5,471,225) in view of Runaldue et al. (US 5,325,338) and further in view of Hoshi (JP 58-143389) and Johary et al. (US 5,196,839).

With respect to claims 9 and 10, Parks, Hoshi and Runaldue disclose, the active matrix display device of claim 6 (see above).

Neither Parks nor Runaldue expressly disclose either a digital or time gradation display device.

Johary discloses, a display device for generating time gradation signals (fig. 1c) and digital gradation signals (fig. 1d).

Johary, Parks, Hoshi, and Runaldue are analogous art because they are all from the same field of endeavor namely display control circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art at the time of the invention to drive the display of Parks and Runaldue under either time or digital gradation signals as taught by Johary.

The motivation for doing so would have been to provide effective visual differentiation for displayed images (Johary; col. 1, lines 28-32).

7. Claims 12-14, 17, 20-21, 24-27, 29, 48 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parks (US 5,471,225) in view of Hoshi (JP 58-132289) and further in view of Johary et al. (US 5,196,839).

With respect to claim 12, Parks discloses, an active matrix display device (fig. 2; col. 3, lines 17-19) having an electro-optical modulating layer (40 in fig. 3) disposed between a pair of substrates (24 and 22 in fig. 2), said active matrix display device comprising:

a plurality of column lines (32 in fig. 5) and a plurality of row lines (34 in fig. 5) supported by one of the substrates (fig. 3) and defining a plurality of pixels in a matrix form (fig. 5);

a plurality of pixel electrodes formed in said plurality of pixels (36 in fig. 5) and supported by said one of said substrates (fig. 3);

a first thin film transistor (col. 3, lines 6-8) disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines (38 in fig. 5);

a memory circuit (52, 54, R1-2 in fig. 5) disposed in each of said pixels and electrically connected to said thin film transistor (fig. 5), wherein said memory circuit stores an information output by said thin film transistor (col. 6, lines 5-18); and

at least two voltage source lines electrically connected to said memory circuit (Power and ground voltages in fig. 5); and

an opposite electrode on the other of said substrates (30 in fig. 3, for example),

wherein different voltages are applied to said pixel electrodes through said at least two voltage source lines based on the information stored by the corresponding memory circuit (col. 6, lines 5-18, 52-61); and

and wherein said memory circuit comprises at least second and third thin film transistors (52 and 54 in fig. 5), one of source or drain of the second thin film transistor being connected with one of said voltage source lines (upper terminal of TFT 54 is connected to power in fig. 5), a gate electrode of the third thin film transistor (upper terminal of 54 is connected to gate of 52), and one of source or drain of the first thin film transistor (upper terminal of 54 is connected to 38 in fig. 5),

the other of source or drain of the second transistor being connected with the other of said voltage source lines (lower terminal of TFT 54 is connected to ground in fig. 5) and one of source or drain of the third thin film transistor (lower terminal of both 52 and 54 are both connected to ground), and

a gate electrode of the second thin film transistor being connected with the other of source or drain of the third thin film transistor, one of said voltage source lines, and said pixel electrode (fig. 5).

Parks does not expressly disclose wherein an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode.

Hoshi discloses, wherein an AC voltage (12a in fig. 3a) having an amplitude equivalent to that of the voltages output of the memory circuit (12b in fig. 3b; both have an amplitude of V) is supplied to the opposite electrode (fig. 2; 8th line from bottom of page 5 of provided translation).

Hoshi and Parks are analogous art because they are both from the same field of endeavor namely LCD device control and driving.

At the time of the invention it would have been obvious to one of ordinary skill in the art to apply the AC voltage as taught by Hoshi for the benefit of reduced power consumption (Hoshi; middle of page 6).

Neither Hoshi nor Parks expressly disclose a time gradation display device.

Johary discloses, a display device for generating time gradation signals (fig. 1c) and digital gradation signals (fig. 1d).

Hoshi, Johary and Parks are analogous art because they are both from the same field of endeavor namely display control circuitry design.

At the time of the invention it would have been obvious to one of ordinary skill in the art at the time of the invention to drive the display of Parks using time gradation signals as taught by Johary.

The motivation for doing so would have been to provide effective visual differentiation for displayed images (Johary; col. 1, lines 28-32).

With respect to claim 13, Parks, Hoshi and Johary disclose, the active matrix display device of claim 12 (see above).

Hoshi further discloses, wherein a voltage supplied to the electro-optical modulating layer is substantially zero on time average (13a in figs. 3a-b is the voltage supplied to the electro-optical modulating layer and is clearly zero on time average).

With respect to claim 14, Parks, Hoshi and Johary disclose, the active matrix display device of claim 12 (see above).

Parks further discloses, wherein the number of pixel electrodes equals the number of the digital memory circuits (clear from fig. 5).

With respect to claim 17, Parks, Hoshi and Johary disclose, the active matrix display device of claim 12 (see above).

Parks, further discloses, wherein the different voltages include a high voltage and a low voltage (fig. 5, power and ground are seen as a high and low voltage).

With respect to claims 20-21, Parks and Hoshi disclose, the active matrix display device of claim 18 (see above).

Neither Hoshi nor Parks expressly disclose either a digital or time gradation display device.

Johary discloses, a display device for generating time gradation signals (fig. 1c) and digital gradation signals (fig. 1d).

At the time of the invention it would have been obvious to one of ordinary skill in the art at the time of the invention to drive the display of Parks using time or digital gradation signals as taught by Johary.

The motivation for doing so would have been to provide effective visual differentiation for displayed images (Johary; col. 1, lines 28-32).

With respect to claim 24, Parks discloses, an active matrix display device (fig. 2; col. 3, lines 17-19) having an electro-optical modulating layer (40 in fig. 3) disposed between a pair of substrates (24 and 22 in fig. 2), said active matrix display device comprising:

a plurality of column lines (32 in fig. 5) and a plurality of row lines (34 in fig. 5) supported by one of the substrates (fig. 3) and defining a plurality of pixels in a matrix form (fig. 5);

a plurality of pixel electrodes formed in said plurality of pixels (36 in fig. 5) and supported by said one of said substrates (fig. 3);

a first thin film transistor (col. 3, lines 6-8) disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines (38 in fig. 5);

a memory circuit (52, 54, R1-2 in fig. 5) disposed in each of said pixels and electrically connected to said thin film transistor (fig. 5), wherein said memory circuit stores an information output by said thin film transistor (col. 6, lines 5-18); and

at least two voltage source lines electrically connected to said memory circuit (Power and ground voltages in fig. 5); and

an opposite electrode on the other of said substrates (30 in fig. 3, for example),

wherein different voltages are applied to said pixel electrodes through said at least two voltage source lines based on the information stored by the corresponding memory circuit (col. 6, lines 5-18, 52-61); and

wherein said memory circuit comprises at least two thin film transistors (52 and 54 in fig. 5), having a same conductivity type (fig. 5).

Parks does not expressly disclose wherein an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode.

Hoshi discloses, wherein an AC voltage (12a in fig. 3a) having an amplitude equivalent to that of the voltages output of the memory circuit (12b in fig. 3b; both have an amplitude of V) is supplied to the opposite electrode (fig. 2; 8th line from bottom of page 5 of provided translation).

Hoshi and Parks are analogous art because they are both from the same field of endeavor namely LCD device control and driving.

At the time of the invention it would have been obvious to one of ordinary skill in the art to apply the AC voltage as taught by Hoshi for the benefit of reduced power consumption (Hoshi; middle of page 6).

Neither Hoshi nor Parks expressly disclose a time gradation display device.

Johary discloses, a display device for generating time gradation signals (fig. 1c) and digital gradation signals (fig. 1d).

At the time of the invention it would have been obvious to one of ordinary skill in the art at the time of the invention to drive the display of Parks using time gradation signals as taught by Johary.

The motivation for doing so would have been to provide effective visual differentiation for displayed images (Johary; col. 1, lines 28-32).

With respect to claim 25, Parks, Hoshi and Johary disclose, the active matrix display device of claim 24 (see above).

Hoshi further discloses, wherein a voltage supplied to the electro-optical modulating layer is substantially zero on time average (13a in figs. 3a-b is the voltage supplied to the electro-optical modulating layer and is clearly zero on time average).

With respect to claim 26, Parks, Hoshi and Johary disclose, the active matrix display device of claim 24 (see above).

Parks further discloses, wherein the number of pixel electrodes equals the number of the memory circuits (fig. 5).

With respect to claim 27, Parks, Hoshi and Johary disclose, the active matrix display device of claim 24 (see above).

Johary further discloses, wherein the active matrix display device includes a digital gradation display device (fig. 1c).

With respect to claim 29, Parks, Hoshi and Johary disclose, the active matrix display device of claim 24 (see above).

Parks, further discloses, wherein the different voltages include a high voltage and a low voltage (fig. 5, power and ground are seen as a high and low voltage).

With respect to claim 48, Parks, Hoshi and Johary disclose, the active matrix display device according to claim 12 (see above).

Parks further discloses, wherein said electro-optical modulating layer comprises a liquid crystal (title).

With respect to claim 50, Parks, Hoshi and Johary disclose, the active matrix display device according to claim 24 (see above).

Parks further discloses, wherein said electro-optical modulating layer comprises a liquid crystal (title).

Conclusion

8. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on June 11th, 2010 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM L. BODDIE whose telephone number is (571)272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/William L Boddie/
Examiner, Art Unit 2629
9/8/2010